

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Currently Amended) A thin film transistor comprising:
2 a buffer layer formed on a substrate;
3 an activation layer formed on said buffer layer; and
4 a gate insulation layer formed on said substrate including said activation layer,
5 with said buffer layer having a step formed between a lower part of said activation layer and
6 a part except said lower part of said activation layer, and said step being a half or less of the
7 thickness sum of said activation layer and gate insulation layer,
8 said buffer layer has a step to such a degree that thickness of said gate insulation layer is not
9 changed on said side wall of said buffer layer.

Claims 2-4. (Cancelled)

1 5. (Currently Amended) The thin film transistor according to claim [[2]] 1, wherein said
2 activation layer being a ~~solid-phase crystallization~~ polysilicon, and a thickness of the gate insulation
3 layer is 400 Å or more when a thickness of said ~~solid-phase crystallization~~ polysilicon is 300 Å and
4 step is 350 Å in said activation layer.

1 6. (Currently Amended) The thin film transistor according to claim [[2]] 1, wherein said
2 activation layer being an ~~excimer laser annealing~~ polysilicon, and thickness of the gate insulation
3 layer is 1,000 Å or more when a thickness of said ~~excimer laser annealing~~ polysilicon is 500 Å and
4 step is 750 Å in said activation layer.

1 7. (Withdrawn) A method for fabricating said thin film transistor of claim 1, comprising the
2 steps of:
3 depositing an amorphous silicon layer on a substrate equipped with buffer layer;
4 forming a polycrystalline silicon layer by crystallizing said amorphous silicon layer;
5 forming an activation layer by etching said polycrystalline silicon layer;
6 treating the surface of said activation layer; and
7 depositing a gate insulation layer on said substrate,
8 with etching time being controlled in said activation layer forming process and activation
9 layer surface treatment process so that step between a lower part of gate in the buffer layer and a part
10 except the lower part of said gate has a step value corresponding to a half or less of the thickness sum
11 of said activation layer and gate insulation layer.

1 8. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,
2 wherein the etching time is controlled so that said buffer layer has a step to such a degree that
3 thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

1 9. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,
2 wherein the etching time is controlled to accommodate said buffer layer having a step corresponding
3 to a half or less of the thickness sum of the activation layer and gate insulation layer.

1 10. (Withdrawn) The method for fabricating a thin film transistor according to claim 9,
2 wherein the etching time is controlled so that said buffer layer has a step to such a degree that
3 thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

1 11. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,
2 wherein a thickness of said gate insulation layer is 400 Å or more when the thickness of solid-phase
3 crystallization polysilicon is 300 Å and step is 350 Å in said activation layer.

1 12. (Withdrawn) The method for fabricating a thin film transistor according to claim 7,
2 wherein thickness of said gate insulation layer is 1,000 Å or more when the thickness of excimer
3 laser annealing polysilicon is 500 Å and step is 750 Å in said activation layer.

1 13. (Currently Amended) A thin film transistor, comprising:
2 a buffer layer;
3 an activation layer formed on said buffer layer; and
4 a gate insulation layer formed on said buffer layer and said activation layer,

5 with said buffer layer having a step formed between a lower part of said activation layer and
6 a part except said lower part of said activation layer, and said step being up to a half of the thickness
7 sum of said activation layer and gate insulation layer,

8 said step being controlled according to said gate insulation layer being deposited to an even
9 thickness on a side wall of said activation layer.

Claim 14. (Cancelled)

1 15. (Currently Amended) The thin film transistor according to claim 13, with said activation
2 layer comprising a ~~solid-phase crystallization~~ polysilicon, and a thickness of said gate insulation
3 layer being at least 400 Å when a thickness of said ~~solid-phase crystallization~~ polysilicon is 300 Å
4 and step is 350 Å in said activation layer.

1 16. (Currently Amended) The thin film transistor according to claim 13, with said activation
2 layer comprising ~~an excimer laser annealing~~ a polysilicon, and a thickness of said gate insulation
3 layer being at least 1,000 Å when a thickness of said ~~excimer laser annealing~~ polysilicon is 500 Å
4 and step is 750 Å in said activation layer.

Claims 17-20. (Cancelled)

1 21. (Previously Presented) The thin film transistor according to claim 1, wherein a thickness

2 of the gate insulation layer is at least 400 Å when a thickness of said activation layer is 300 Å and
3 step is 350 Å in said activation layer.

1 22. (Currently Amended) The thin film transistor according to claim 1, wherein the step of
2 said buffer layer being formed on a single body of said buffer layer with the step protruding from a
3 flat portion of said buffer layer ~~and the step of said activation layer being formed on a single body~~
4 ~~of said activation layer with the step of said activation layer protruding from a flat portion of said~~
5 ~~activation layer.~~